tinyGTC GPSDO

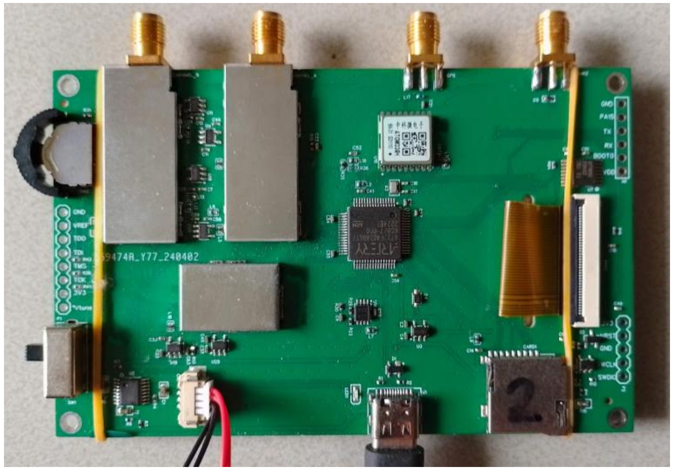
Component Options, System Design, Simulation and Validation

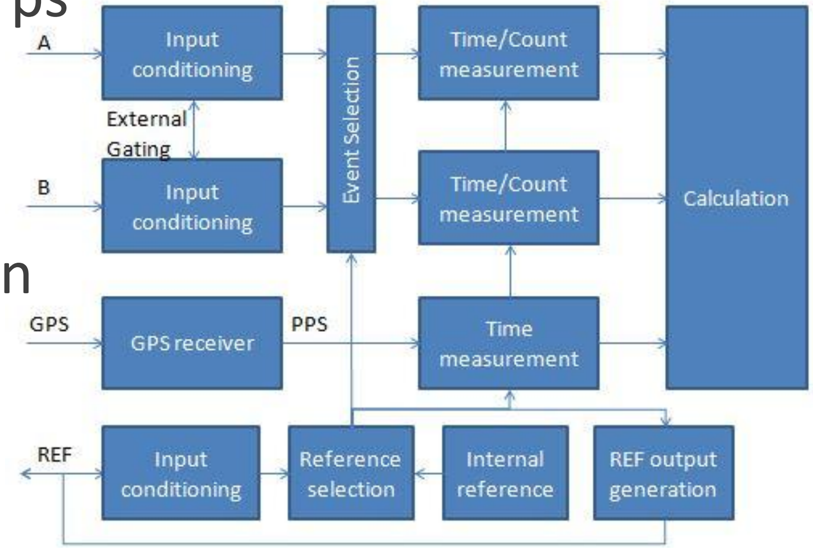
Content

- tinyGTC and its internal reference
- Problem: Oscillator (in)Stability
- Solution: GPS time/frequency transfer
- Design: Components and Architecture
- Simulation
- Validation

What is a tinyGTC?

- A Dual channel, Reciprocal, Interpolating, Linear Regression, Gapless timer/counter with SCPI support.
- 2 input channels:
  - 0.1 Hz to 350 MHz(B) / 6 GHz (A)
  - Accuracy better than 1e-11/s
  - Single shot time resolution of 40 ps
- Internal GPS Disciplined Oscillator
- Reference input/output
  - Output from 0.1 Hz to 300 MHz with 0.01 Hz frequency resolution
- Cheap, small and portable
- Currently starting with beta testing.





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tinyGTC Internal reference

10 MHz reference for time and frequency measurement

Design constraints:

- Cost : Must be fraction of total cost. (<5$)
- Size: Has to fit on SMD PCB in small enclosure.
- Power consumption: Allow at least 5 hours battery life.
- Speed: Frequency error below 1e-9 within 1 minute
- Stability: Preferably matching with tinyGTC accuracy of 1e-11

Presenting oscillator stability
Understanding ADEV

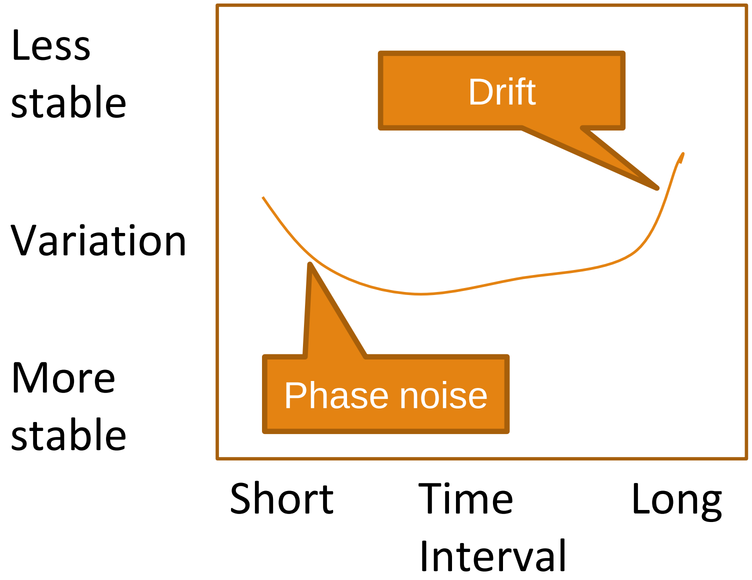
- Allan Deviation (ADEV) computes the
  - **Average difference (Variation)** of two measurements versus the
  - **Time interval** between the two measurements

- Often plotted in Log-Log scale of Variation versus Time Interval
- The level of Variation can also be called the level of Stability

- ADEV number is meaningless without mentioning the interval at which it is measured

- ADEV = 1e-10 @ 1 s means:
  - Average 1e-10 variation
  - When measured over a 1 s interval
- ADEV can also be used for a counter
  - Specifies measurement error
  - 1e-10 @ 1 s = 10 digits / s
  - Reality is more complex

Some examples:



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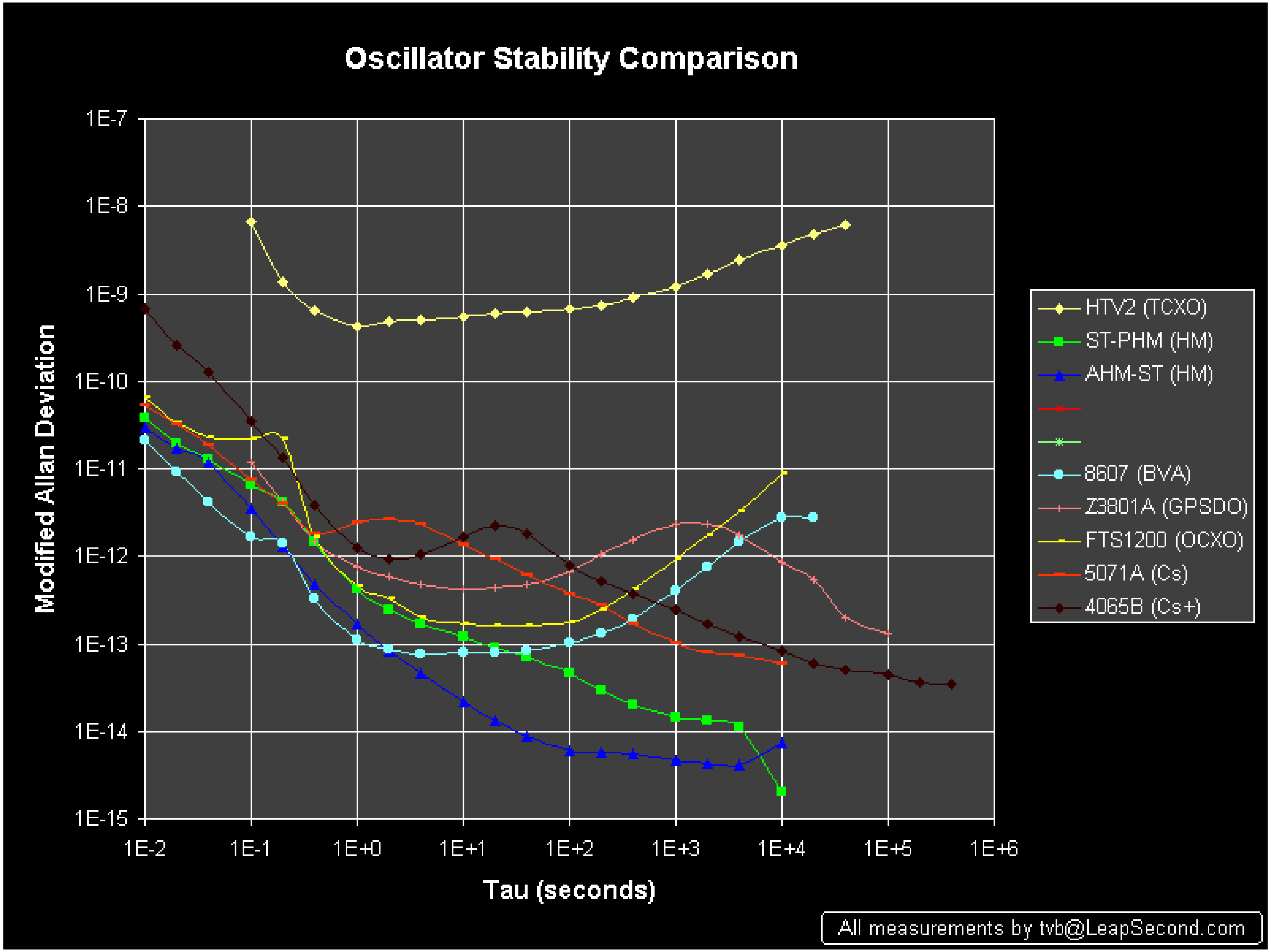
Typical stability of oscillators



TCXO
H2 Maser
H2 Maser

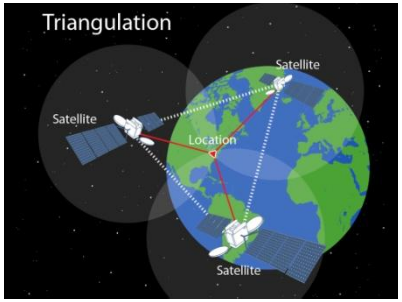
OCXO
GPSDO
OCXO
Cesium beam
Cesium beam

Long term stability of oscillators

Technology	Stability	Up to	Power	Cost
XO	1e-6 to 1e-7 @ 1 s	10 s	0.01 W	0.5 $
TCXO	1e-9 to 1e-10 @ 1s	100 s	< 0.1 W	1 $
OCXO	1e-10 to 1e-12 @ 1s	1000 s	3 W	25 $
Rubidium	1e-13 @ 1 day	1e-11 / month	15 W	400 $
Cesium	1e-14 @ 1 day	<< 1e -11 / month	40 W	1500 $
H Maser	1e-15 @ 1 day	<< 1e-11 / month	500 W (?)	> 100 k$

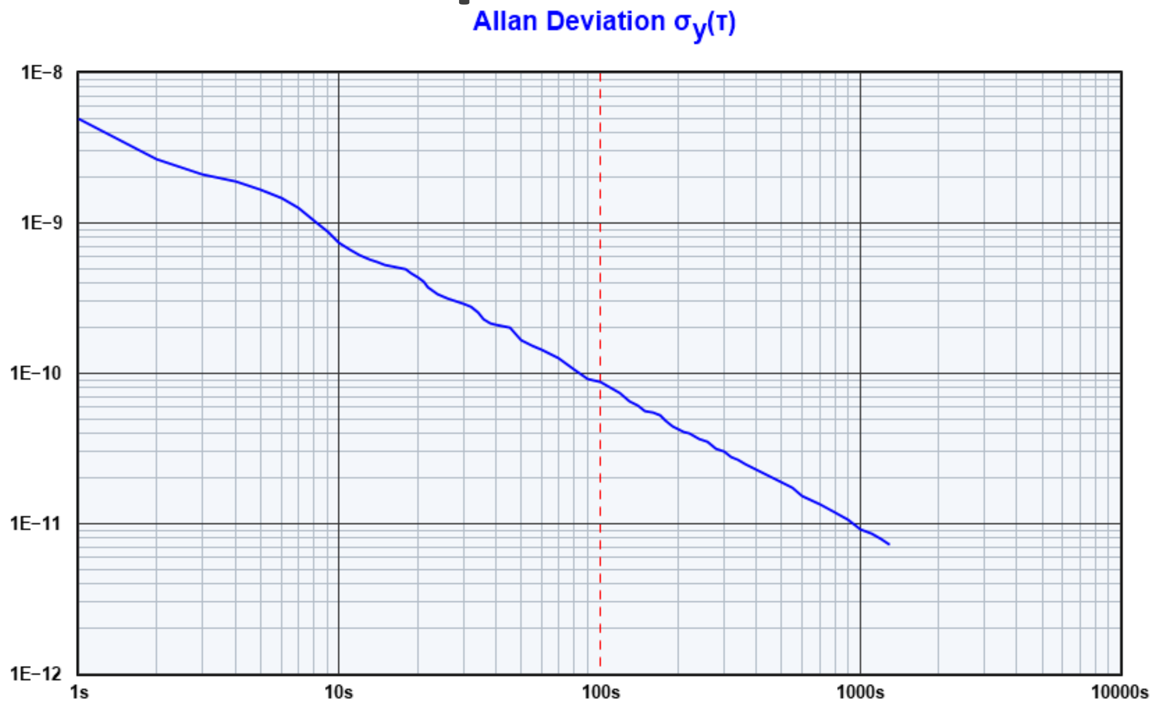
- Long term drift is the biggest limitation with cheaper oscillators
- If it would be possible to "transfer" time from a remote accurate oscillator to the tinyGTC it would be possible to "adjust" a less accurate oscillator to eliminate the long term instability
- How about GPS?

GPS system



- Each GPS satellite contains a Cesium clock, synced to common “GPS” time, and broadcasts its time and position.
- Positioning of GPS receiver based on triangulation to at least 3 satellites using difference of received time due to speed of radio waves and distance to satellite.
- GPS receiver can also calculate the “GPS” time and output a pulse at the start of each “GPS” time second
- Measuring the “any output frequency” requires some extra HW for a 3rd frequency counter to have similar accuracy as PPS
- Can this timestamp/frequency be used to discipline a oscillator?
  - Yes! This is called a GPS Disciplined Oscillator (GPSDO)
  - But what is the quality of this timestamp/frequency?

Typical cheap GPS PPS ADEV



Trace	Notes	Input Freq	Sample Interval	ADEV at 100s	Acquired	Instrument
Chinese GPS		10 MHz	1.000 s	8.80E−11	5257 pts	Picotest/Array U6200A series

- PPS is phase locked to GPS time causing one decade per decade drop of ADEV
  - PPS Stability measured against 1 Hz derived from a Rubidium reference clock
- Up to 20 ns error per measurement period of 1 s equals 5e-8 stability at 1 s
- At 100 s this drops to 1e-10, equal to TCXO stability.
- What is causing the 20 ns error?

GPS time error sources(1)

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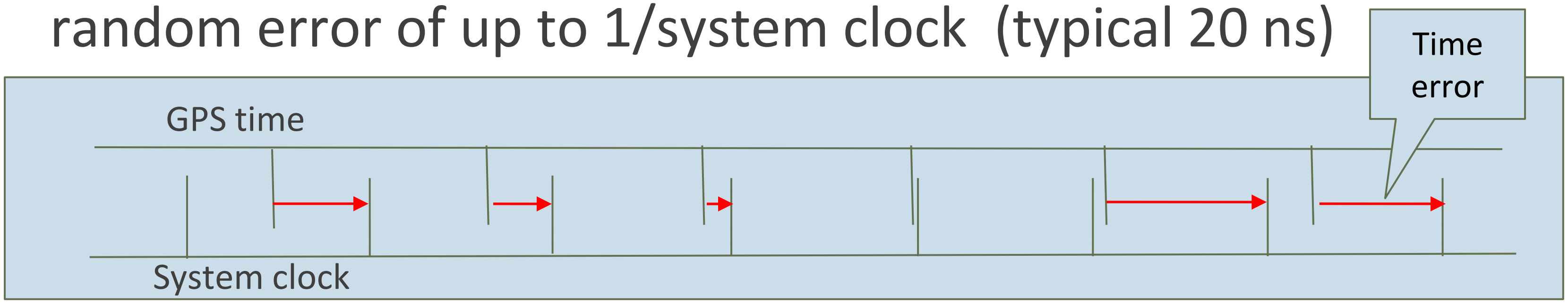
Problem: GPS receiver internal clock frequency:

- The 1 PPS output is derived from internal clock causing a random error of up to 1/system clock (typical 20 ns)



Solution: Communicate time error before outputting next PPS

- PPS receiver subtracts communicated time error.
- Improves ADEV to 1e-11 @ 100 s (factor 10 improvement)
- This is called "Sawtooth correction"

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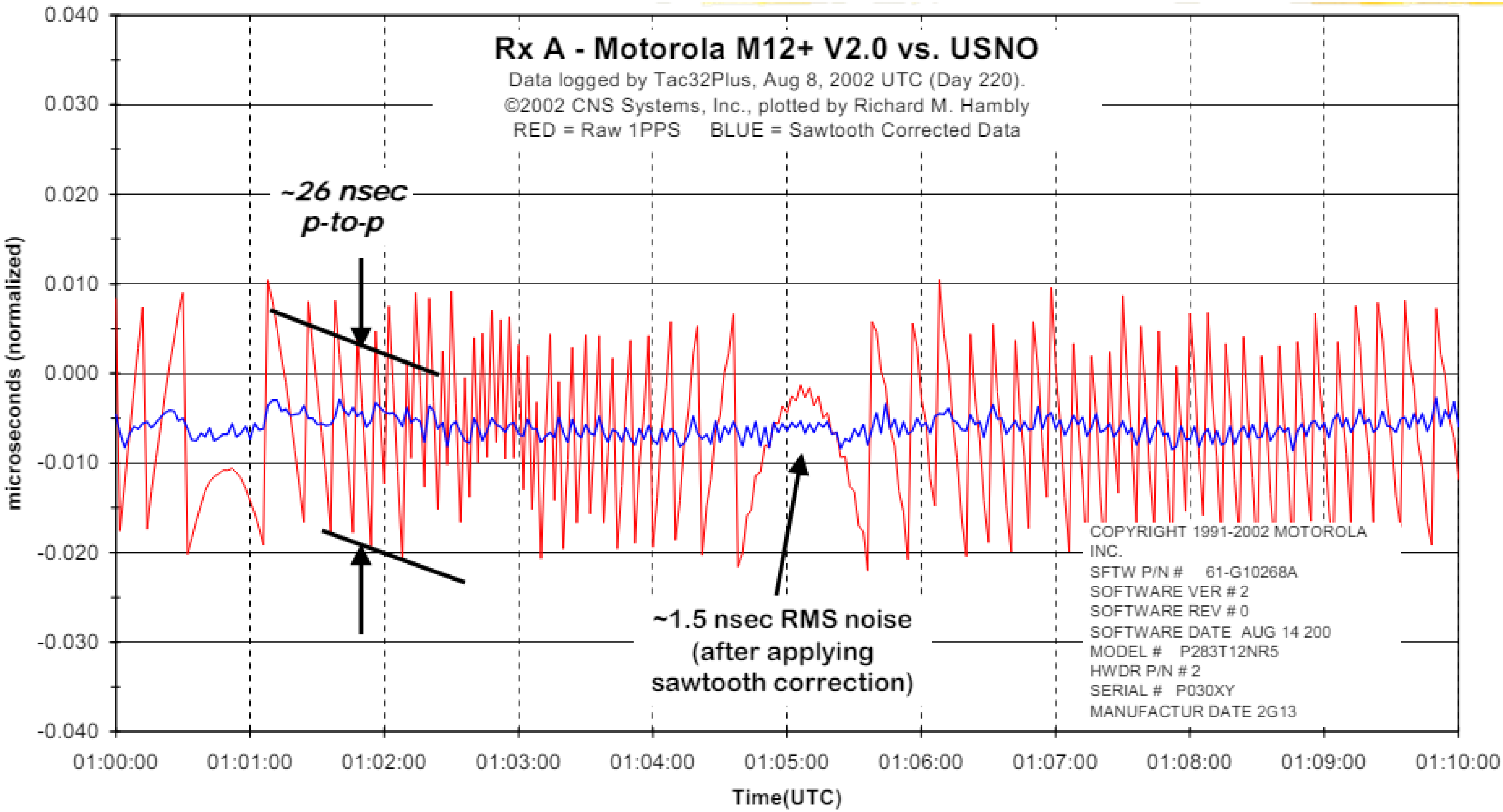
Impact of sawtooth correction



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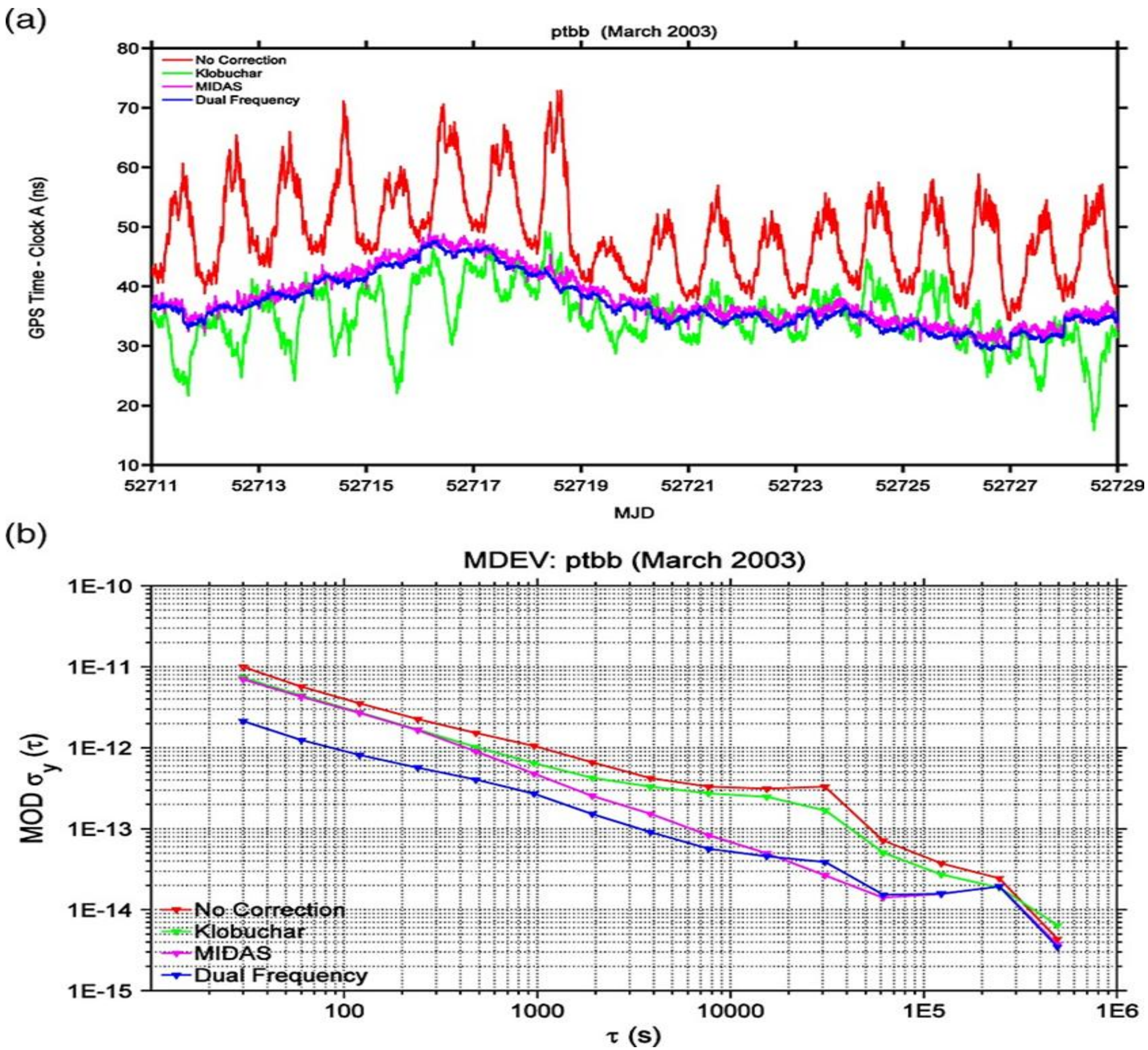
GPS time error sources(2)

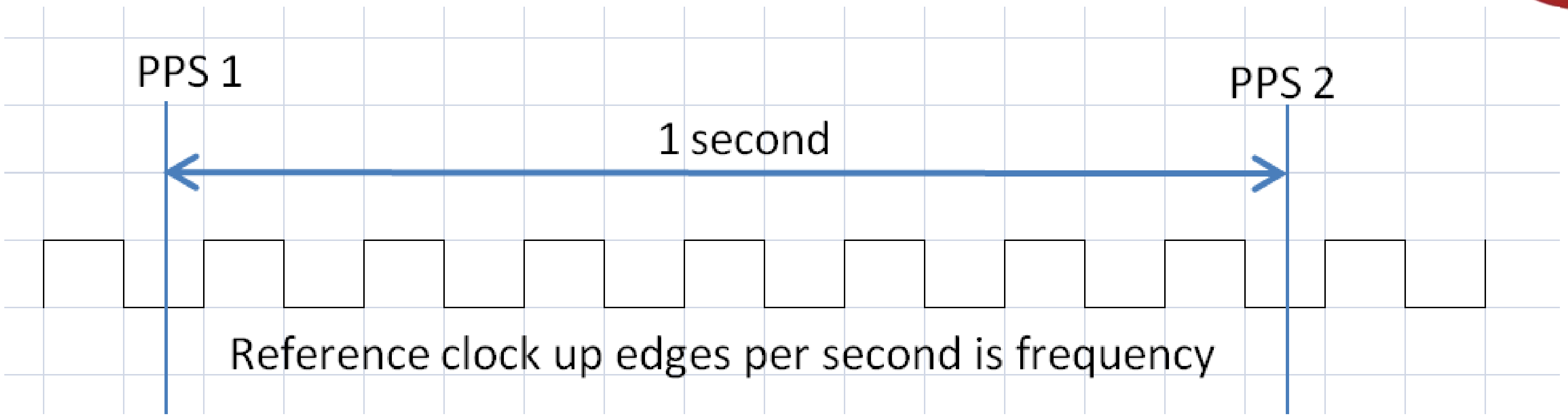
- Problem: Ionosphere delay varies over time.
  - Daily variation up to 20 ns
  - Ionospheric delay depends on transmitter frequency
- Solution: Use multiple frequency bands to eliminate variations
  - Modern GPS satellites transmit on multiple frequencies.
  - Daily variation can be eliminated but not the long term variation (see next slide)

GPS ionosphere delay variation



Good multi band receiver
Can have an ADEV of
1e-12 @ 100 s compared
to 1e-10 @ 100 s for
cheap single band GPS.

How to measure the PPS (1)



Simplest method is to count the amount of reference clock pulses between each PPS pulse

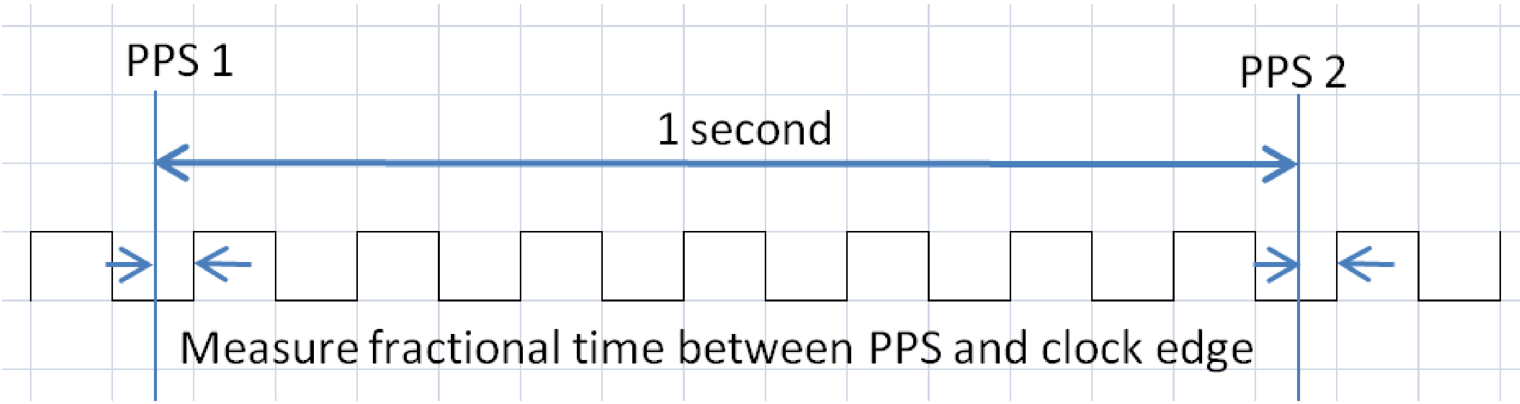
- Reference clock runs at 10 MHz
- Using this clock for time measurements gives 100 ns resolution.
- This increases PPS error from average 20 ns to average 50 ns
- This works with sufficiently long averaging but not good when using a TCXO
- How can we measure PPS more accurately?

How to measure the PPS (2)

Increase reference clock frequency:

- Use PLL to increase reference frequency used to measure time between PPS pulses
- Max frequency depends on IC technology but above 250 MHz (4 ns resolution) will be difficult/expensive.

How to measure the PPS (2)



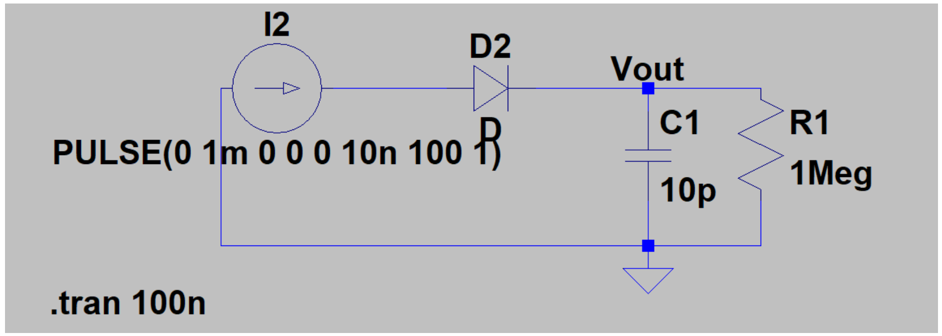
Time between PPS =

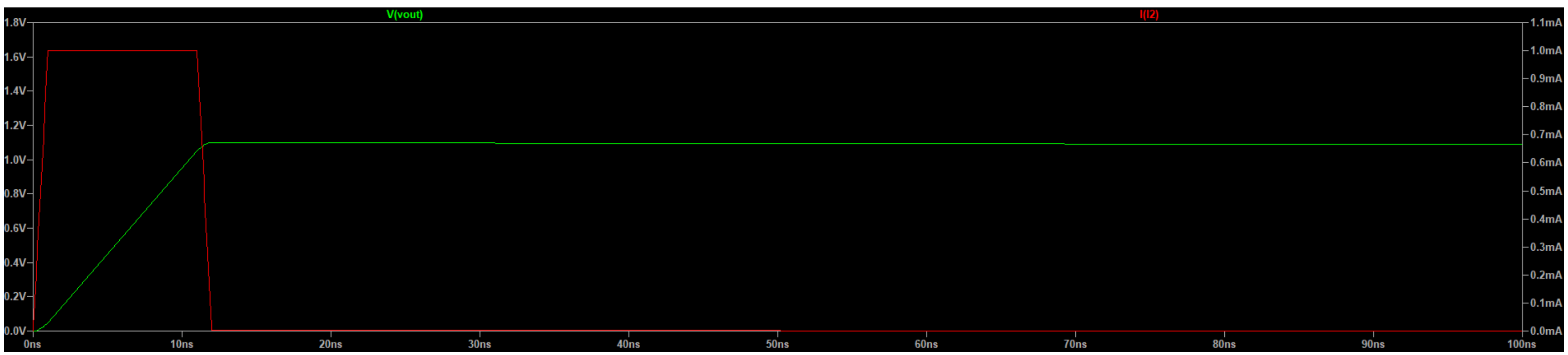
frac1 + (n+1) clock periods – frac2

How to measure this fraction of the clock period?

- Option 1: Analog interpolator
- Option 2: Digital interpolator

Analog interpolator





Method invented by HP for their frequency counters.

Translates short current into constant voltage

What is the possible resolution and accuracy?

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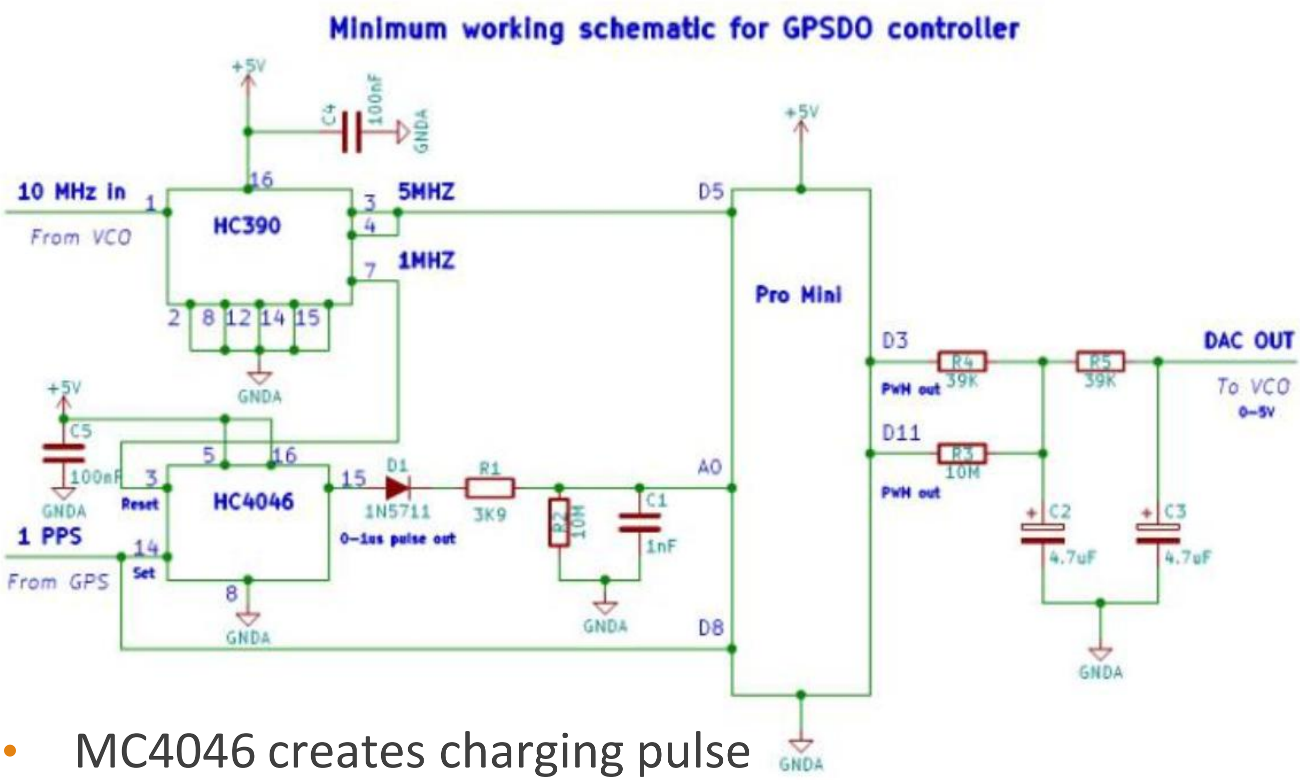
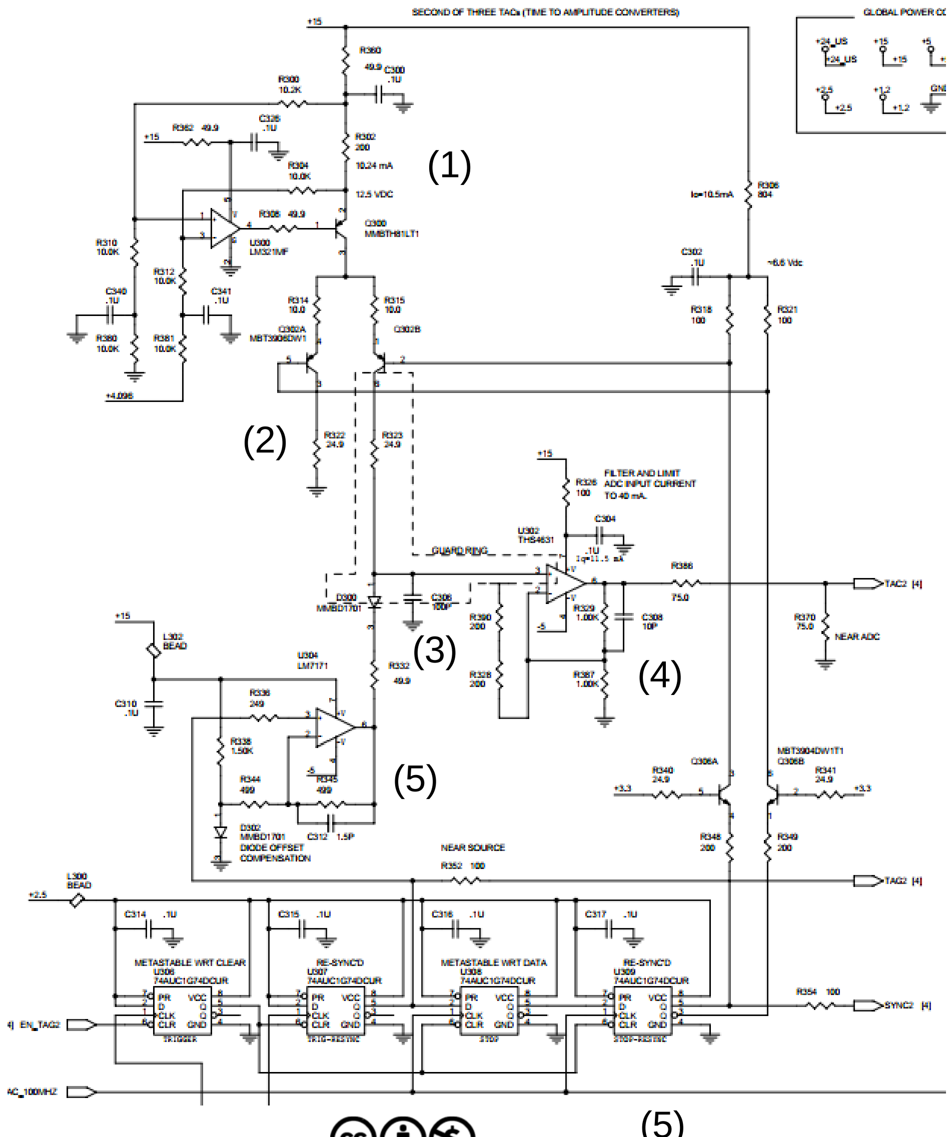
Example 1: LARS GPSDO



- MC4046 creates charging pulse
- Diode + resistor as current source
- ADC of Pro Mini measures voltage
- Resistor over capacitor discharges before next pulse
- 1 ns resolution. 10 ns (?) RMS accuracy

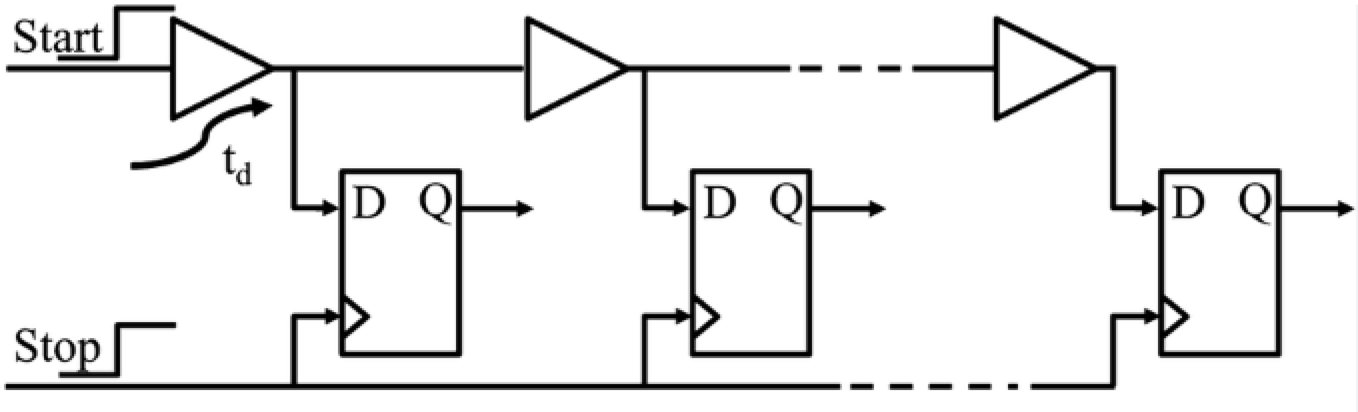
Example 2: FS740



Elements:

- Current source (1)
- Balanced current switch (2)
- Capacitor (3)
- Voltage buffer for ADC (4)
- Discharge circuit (5)
- START/STOP timing generation (6)
- 1 ps resolution and 40 ps RMS accuracy

Digital interpolator



Time to Digital Converter

- Uses a long sequence of logic gates and measures how far the START pulse has propagated through the gates at the STOP pulse.
- Typical per gate delay between 20 ps and 70 ps
- Implemented in one small IC (TDC) and some logic to generate START and STOP
- Requires frequent calibration as gate delay depends on temperature and supply voltage

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Example: TDC7200

- Resolution 55 ps
- STDEV error 35 ps
- Range 12 ns to 500 ns
- SPI interface for data
- Clock for calibration
  - Temperature
  - Voltage

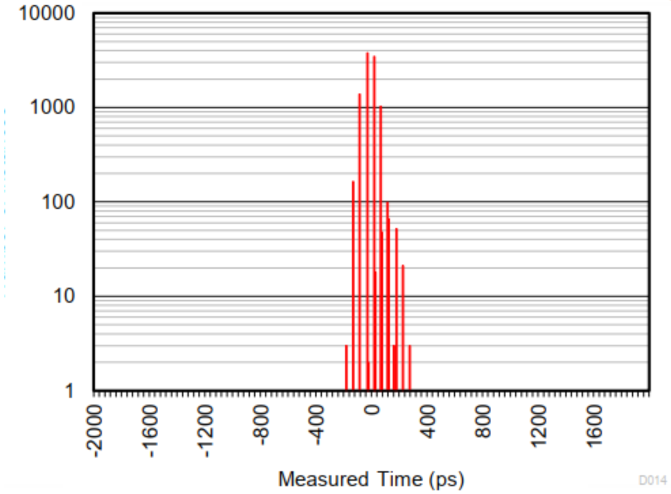
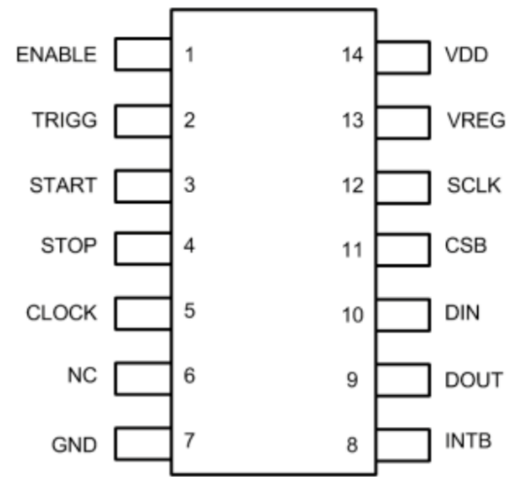


Figure 14. Standard Time-of-Flight Histogram (Normalized)



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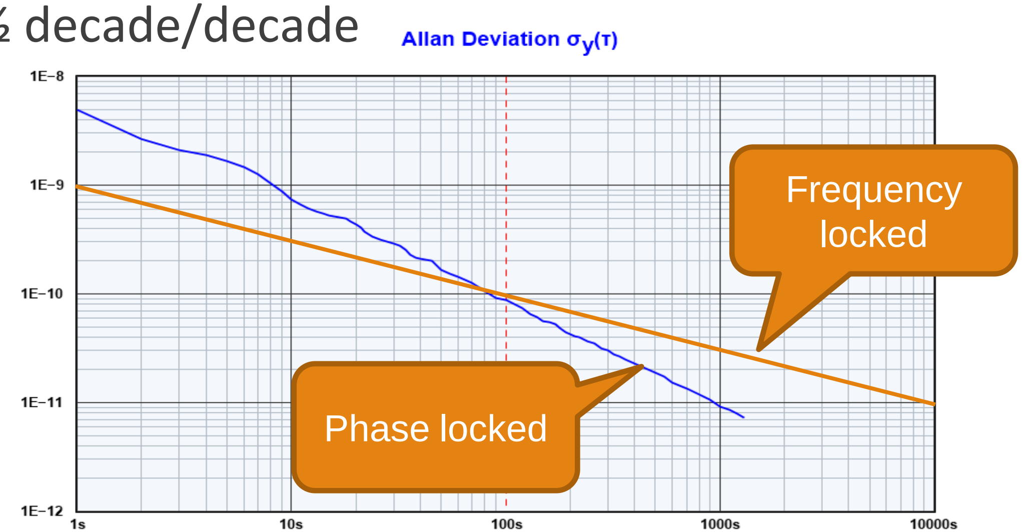
How about using a higher frequency output instead of the PPS?

- Many GPS modules can output “any” frequency using their internal system clock and a fractional divider
- This output can have a lot of jitter due to the fractional divider but may contain more information per second (average over one second possibly solves sawtooth problem)
- No guarantee the frequency output is phase locked to GPS
- Measuring the frequency of this output does not give the decade/decade down slope but only ½ decade/decade



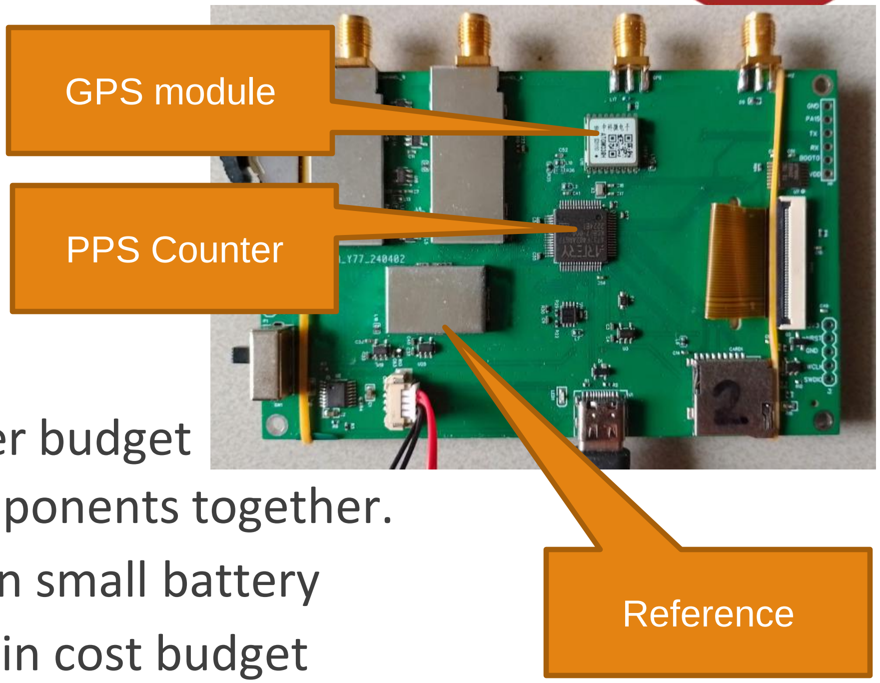
Trace	Notes	Input Freq	Sample Interval	ADEV at 100s	Acquired	Instrument
Chinese GPS		10 MHz	1.000 s	8.80E−11	5257 pts	Picotest/Array U6200A series

Design: Components options

Reference	GPS	PPS measurement
XO	Basic	Count reference
TCXO	Sawtooth correction	Count PLL locked to reference
OCXO	Multiband STcorr	Add analog or digital interpolator

Design: Selected Components

Reference	GPS	PPS measurement
XO	Basic	Count reference
TCXO	Sawtooth correction	Count PLL locked to reference
OCXO	Multiband STcorr	Add analog or digital interpolator



Reference: only TCXO fits in cost/power budget

- OCXO costs most than all other components together.
- OCXO can not operate for 5 hours on small battery

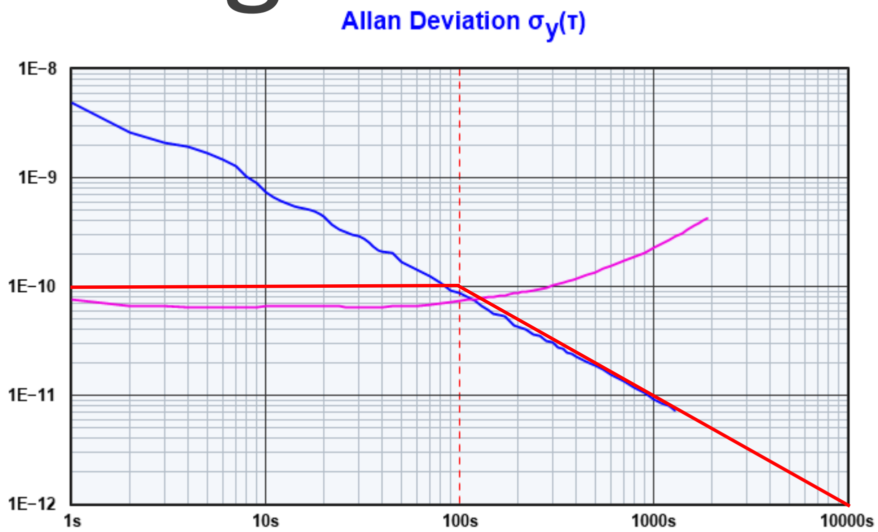
GPS: Only most basic GPS receiver fits in cost budget

- Receiver with Saw tooth correction and/or multi band receiver costs more than all other tinyGTC components together.

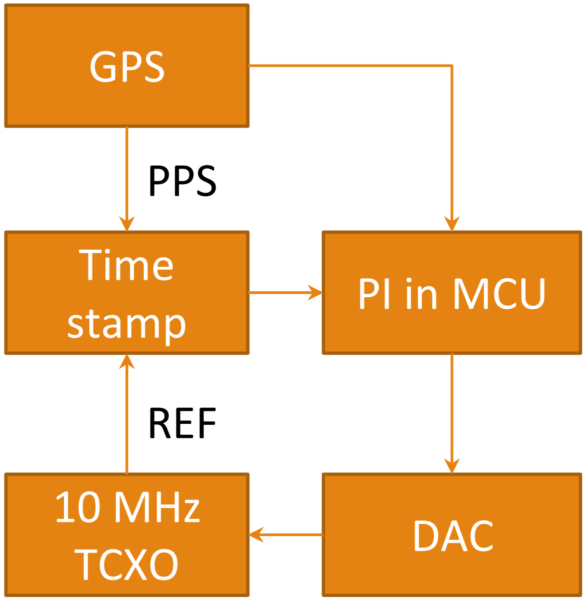
PPS measurement: No fractional measurement

- Use PLL to increase reference clock to 240 MHz
- No fractional time measurement for PPS
- PPS time resolution 4.2 ns, sufficient given 20 ns PPS noise

Design: Architecture



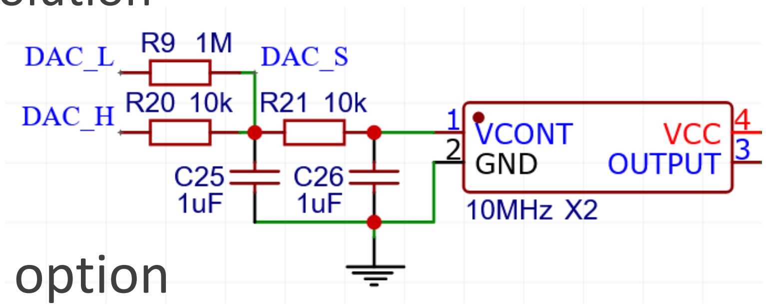
Trace	Notes	Input Freq	Sample Interval	ADEV at 100s	Acquired
Chinese GPS		10 MHz	1.000 s	8.80E−11	5257 pts
tinyGTC unlocked		10 MHz	1.000 s	7.39E−11	7706 pts



- Use internal TCXO oscillator for short term stability (pink trace)
- GPS provides long term stable PPS output (blue trace))
- PPS time stamped using 240 MHz PLL locked to reference
- Use slow PI loop to adjust frequency of the TCXO using a DAC (red trace)
  - Below 100 s TCXO stability dominates
  - Above 100 s GPS time dominates

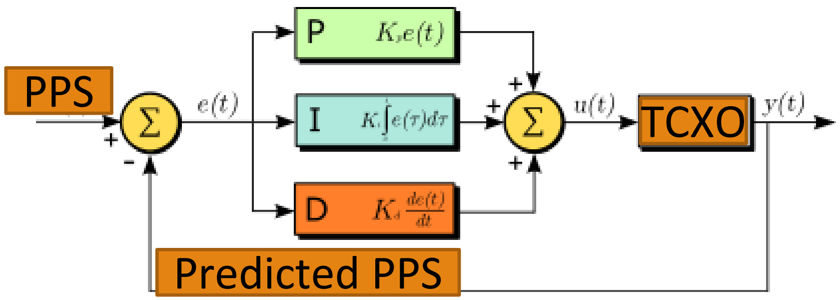
Design: Selecting the DAC

- TCXO control range is 200 Hz for 0-2 V
- With 10 MHz output this equals to 2e-5 variation
- Minimum DAC step must be well below target ADEV
- Full range / Smallest step = Required DAC resolution
- 2e-5 (full range) / 5e-11(target smallest step) = 4e+5
  - Option 1: 16 bit DAC. Not enough resolution
  - Option 2: Summing two 12 bit DAC's
    - Summing ratio 100:1
    - High DAC to reach lock
    - Low DAC once locked



- Quadruple 12 bit DAC is the cheapest option
  - High DAC with 200 Hz range and 5e-9 per step
  - High DAC output noise below 5e-11
  - Low DAC with 2 Hz range and 5e-11 per step
  - Other 2 DAC's used to set counter trigger levels

Design: PI Controller

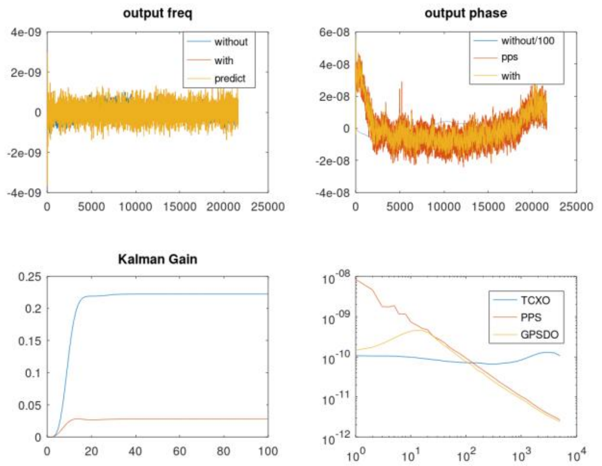


Output Change =
(Proportional (Kp) * Frequency Error +
Integral (Ki) * Phase Error) /
loop_gain(Hz/DAC Step).

- PI controller acts on time difference between predicted PPS time and actual PPS timestamp
- Kd = 0 because of large amount of noise in PPS
- Controller runs every second.
- Problem 1: Kp term causes PPS noise to disturb the TCXO : This noise raises the ADEV below 100 s.
- Solution: Kalman filter before P term can reduce Tau < 100 s noise
    - Not yet implemented
- Problem 2: Measuring ADEV up to 1000 s takes almost one hour
- Solution : Tune Kp and Ki using simulation!

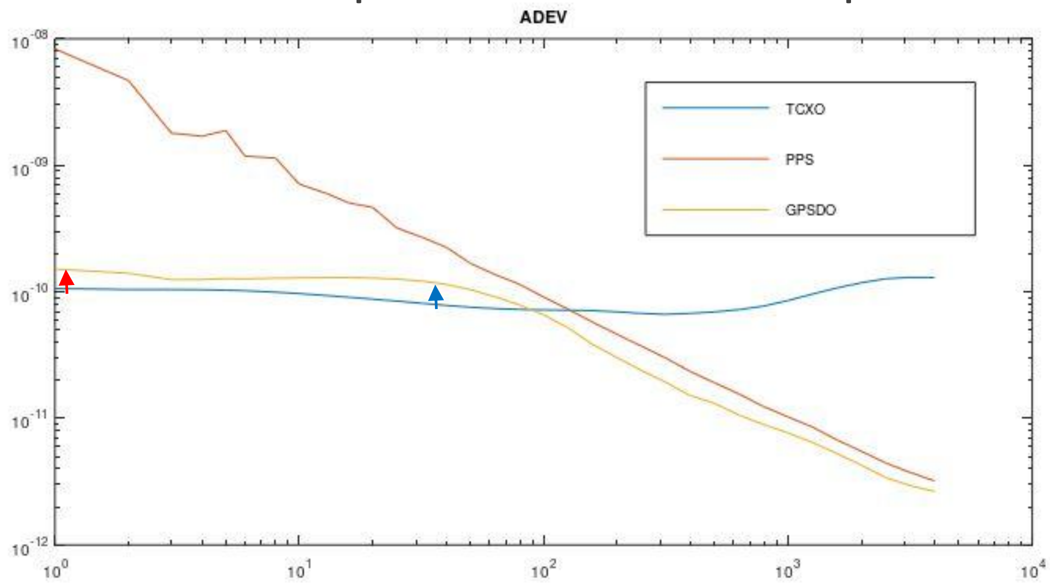
Simulating the PI controller(1)

- Use real measured data as input:
  - 6 hours of GPS PPS measured using Rubidium reference
  - 6 hours of TCXO frequency (un)stability measured using Rubidium as reference
- Convert high resolution measured data to realistic system data
  - Measured PPS is resolution converted to 4 ns
- Control algorithm in simulation implemented with exactly the same resolution as will be used in the target
- DAC resolution simulated by identical quantization of calculated Vtune.
- Controller stability checked by adding a random (both size and timing) jump in input PPS data
- Simulation of 6 hours of running the GPSDO takes about 1 second.
- Various charts generated
  - Output frequency
  - Output phase
  - ADEV
  - Additional controller parameters
- Simulation done in Octave, about 200 lines



Simulating the PI controller(2)

- Simulation output ADEV chart for optimal control parameters



- Optimal PI parameters established (Kp = 0.04, Ki = 0.0001)
- Control “noise” reduces TCXO performance a bit below 100 s (red arrow)
- Small bump (blue arrow) where controller starts to take control is unavoidable
- The above ADEV chart is the benchmark for the actual performance.

Actual control algorithm

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- Measure control gain (Hz per DAC step) for high/low DAC. This takes care of TCXO differences and aging.
- Problem: TCXO initial frequency can be many Hz wrong and a portable GPSDO should quickly reach below 1e-9 frequency error but Kp = 0.04 makes reaching this low error level very slow and Ki will cause a lot of overshoot.
- Solution: Use multiple controllers
  - **Frequency error > PPS noise level (2e-8)**
    - Use frequency error to control frequency using high DAC
    - Kp = 1 and Ki = 0 for very fast reduction of error
    - This quickly drops the error below high DAC step of 5e-9
  - **Frequency error < PPS noise level**
    - Use phase error to control only low DAC
    - Use Kp = 0.04 and Ki = 0.0001
    - This will keep the phase locked to PPS

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System Validation

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System components with their critical requirements:

- GPS: PPS time error below 20 ns
- DAC : Monotonous, noise level, step size
- VC-TCXO + DAC: Frequency resolution/noise
- Total system

Required tools:

Minimum for system level performance:

- Known good Rubidium or better reference
- tinyPFA or very good frequency counter.

Nice to have in case of problems:

- High resolution voltmeter (6.5 digit at least)
- Known very stable OCXO based reference
- High resolution time measurement (1 ns or better)

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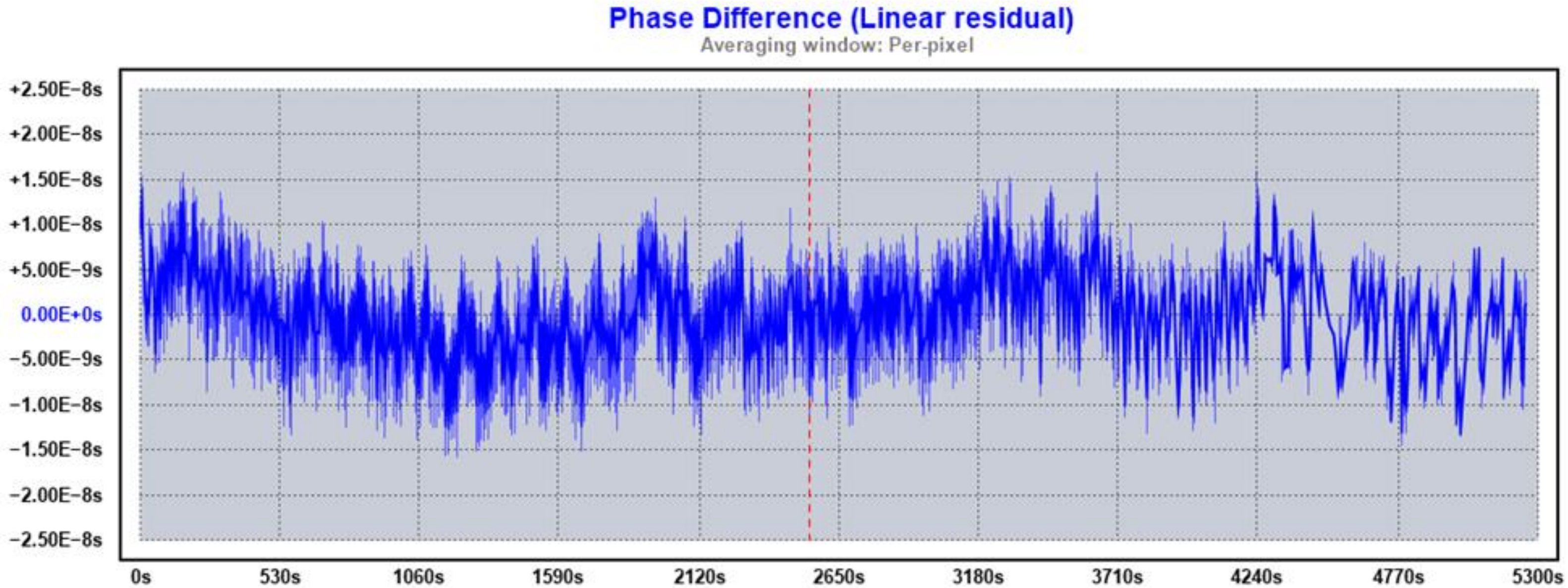
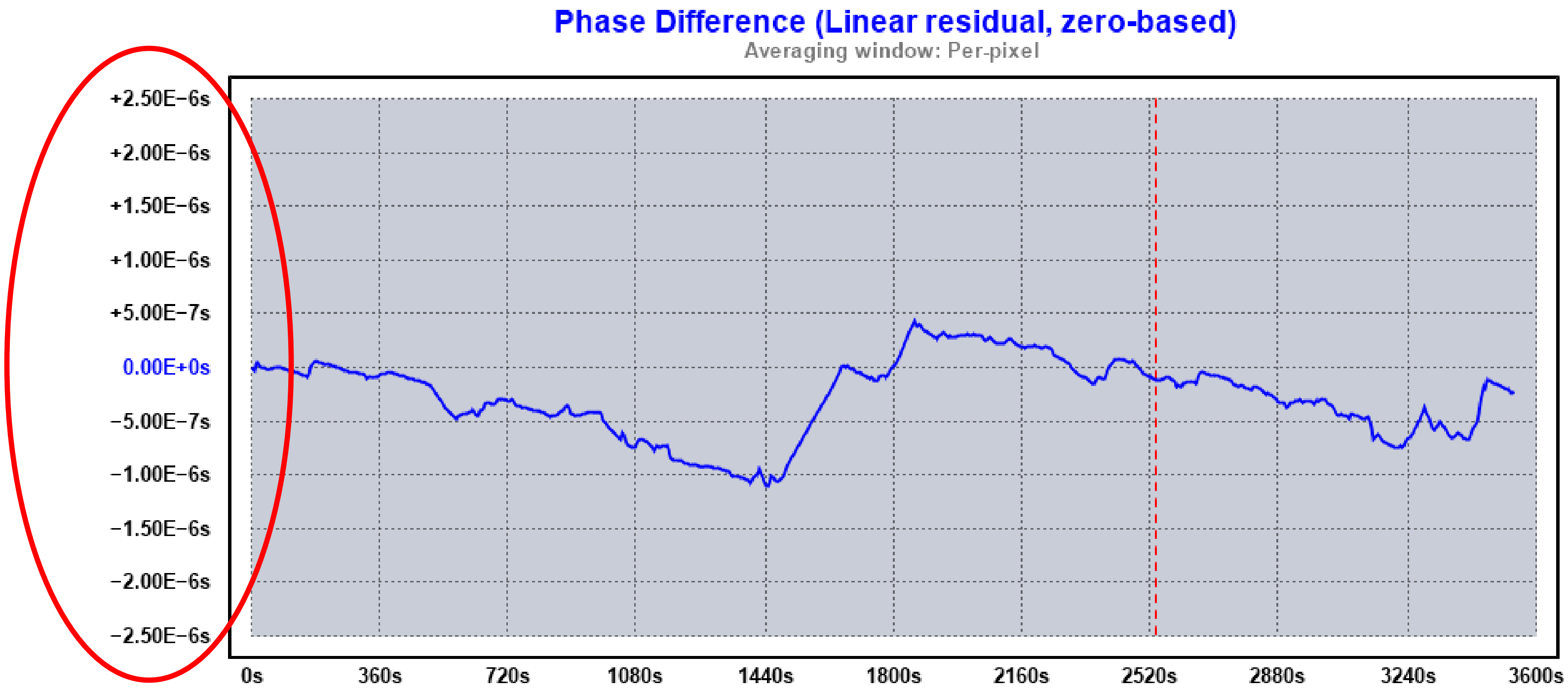
Validating: GPS PPS



Trace	Notes	Input Freq	Sample Interval	Phase at 2536s	Duration	Elapsed	Acquired	Instrument
Chinese GPS		10 MHz	1.000 s	-1.05E-7s	1h 27m 37s	1h 27m 37s	5257 pts	Picotest/Array U6200A series

- ADEV chart is summary. Also need to check phase variations
- GPS PPS phase measured against 1 Hz derived from 10 MHz Rubidium.
- GPS PPS jitter within 20 ns
- Slow phase variations in line with Ionosphere delay variations (20 ns)

Impact of bad antenna signal



Trace	Notes	Input Freq	Sample Interval	Phase at 2536s	Duration	Elapsed	Acquired	Instrument
PPS bad (Unsaved)		10 MHz	1 s	2.27E-6s	58m 58s	58m 58s	3538 pts	PICOTEST

- Factor 10 higher phase variations: 2.5e-7 instead of 2e-8 (see vertical scale)
- Impossible to discipline the TCXO at 100 s and larger

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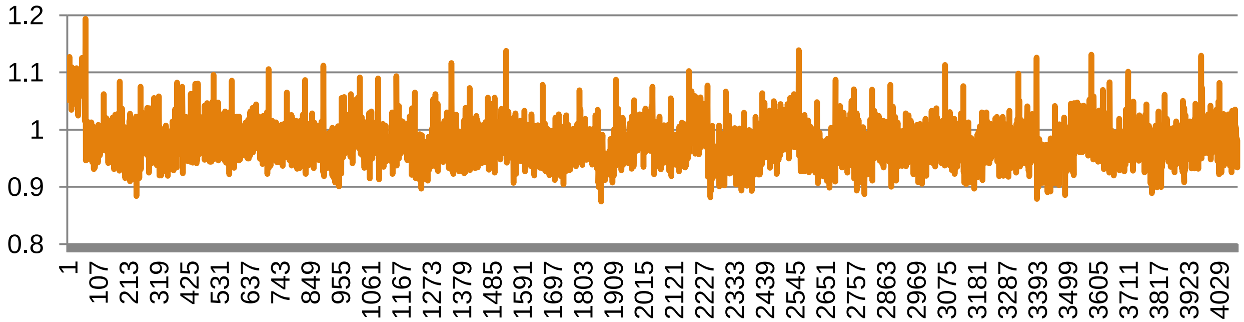
Validating: High DAC(1)

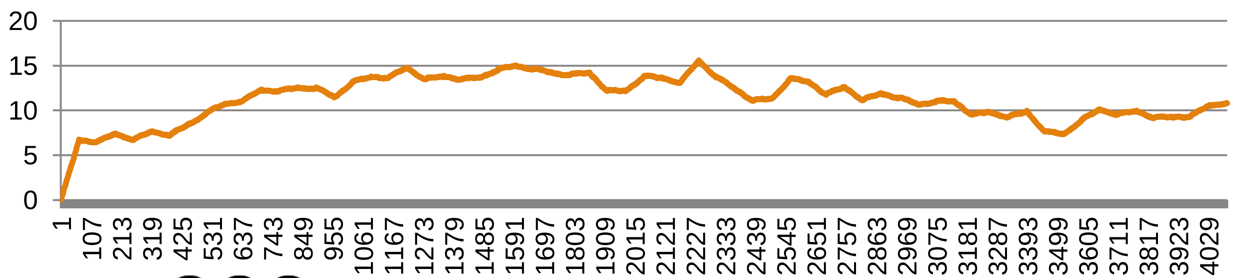
- Step through all DAC output voltage values and check voltage step sizes
  - DAC steps are monotonous

Normalized Step Size



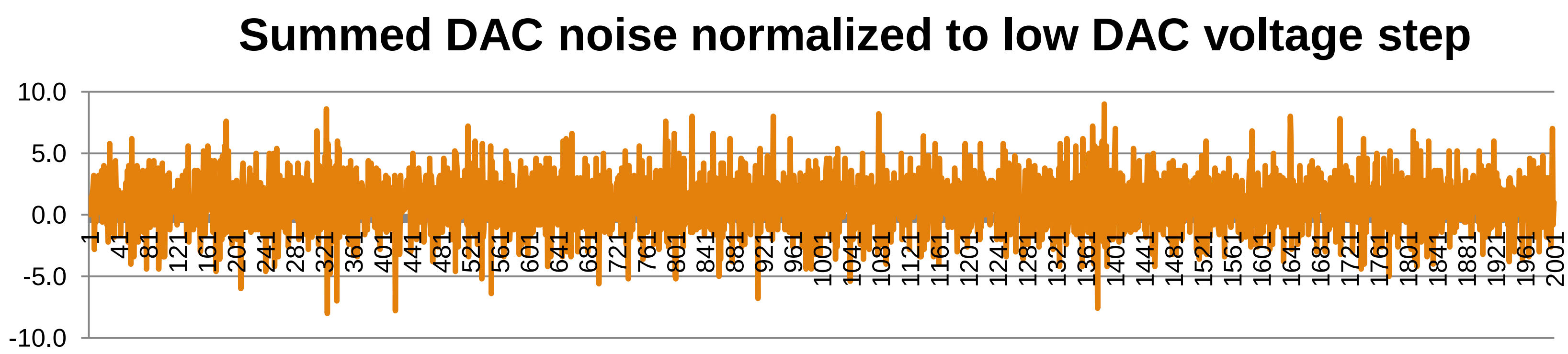
- Check for all DAC output values the deviation from linearity
  - Deviation from linear below 0.2 % securing constant loop gain

Normalized Linear Residue



Validating: High DAC(2)

- Noise level from high output DAC should be low enough compared to low DAC output
  - Voltage noise average 2 low DAC steps, just acceptable



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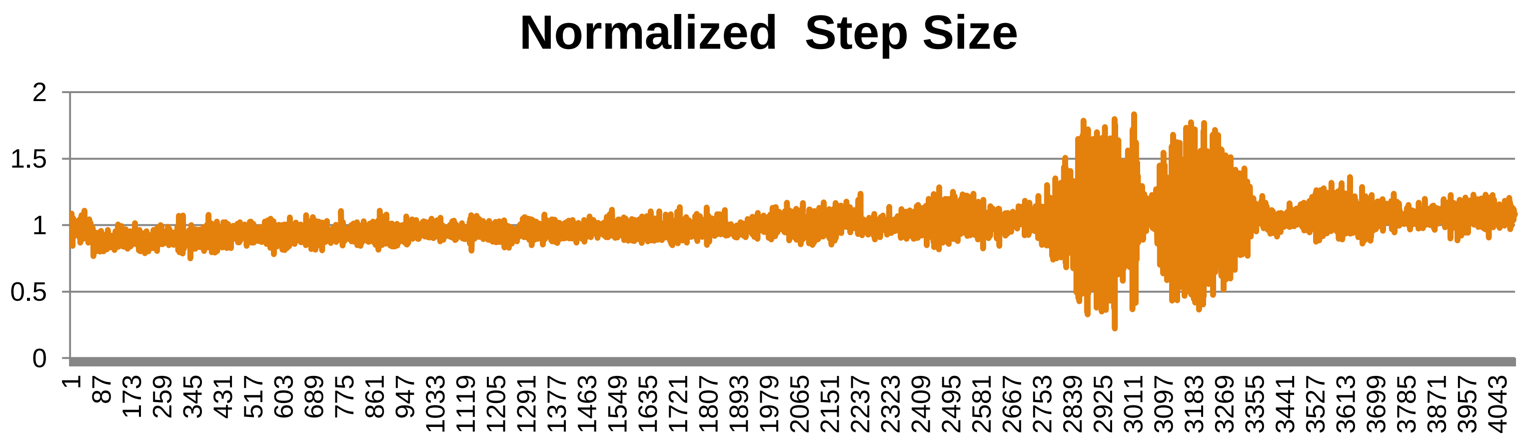
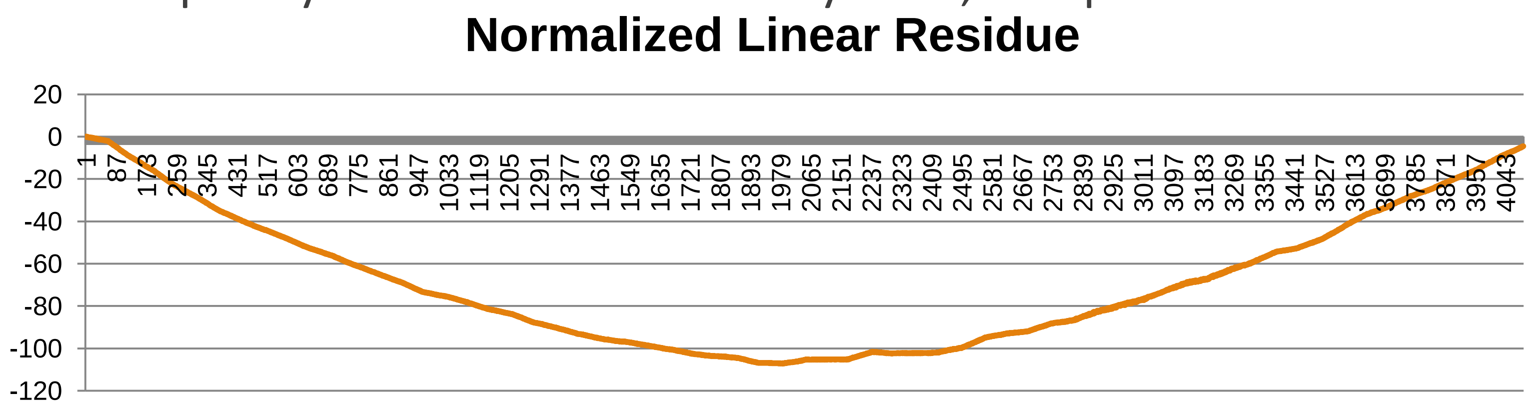
Validating: DAC + VC-TCXO

- Step through all DAC output voltage values and check TCXO frequency step
  - Frequency steps also monotonous



- Check for all DAC output values the deviation from frequency linearity
  - Frequency deviation from linearity 2.5%, acceptable.



Validating: Total system

Trace	Input Freq	Sample Interval	ADEV at 100s	Duration	Elapsed	Acquired	Instrument
PPS (Unsaved)	10 MHz	1.000 s	9.11E-11	5h 13m 32s	5h 13m 32s	18812 pts	Picotest/Array U6200A series
TCXO (Unsaved)	10 MHz	1 s	7.14E-11	5h 43m 18s	5h 43m 18s	20598 pts	
GPSDO kP=0.04	10 MHz	1.000 s	4.27E-11	5h 14m 28s	5h 14m 28s	18868 pts	Picotest/Array U6200A series
GPSDO kP=0.02	10 MHz	1.000 s		4h 8m 50s	4h 8m 50s	14930 pts	Picotest/Array U6200A series

- Green trace is GPSDO performance against a Rubidium reference
- Multiple PI parameters tested to check design robustness
- Phase lock reached within 35 seconds
- Actual performance in line with simulation within statistical uncertainty

Next steps

- Check if jump recovery needs third control algorithm.
  - Something in between the fast and slow loop
- Check stability at various temperatures
  - Winter conditions versus Summer conditions.
  - (Very) Cold start
- Check for impact of other electronics on the board
- Suggestions?

Questions

?

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